ABSTRACT

A circuit operable to measure leakage current in a Dynamic Random Access Memory (DRAM) is provided comprising a plurality of DRAM bit cell access transistors coupled to a common bit line, a common word line, and a common storage node, wherein said access transistors may be biased to simulate a corresponding plurality of inactive bit cells of a DRAM; and a current mirror in communication with the common storage node operable to mirror a total leakage current from said plurality of bit cell access transistors when the access transistors are biased to simulate the inactive bit cells.